WHAT IS CLAIMED IS:

1. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly on a substrate by using a first mask, the gate line assembly including gate lines, gate electrodes, and gate pads;

depositing a gate insulating layer, a semiconductor layer, a contact layer, and a first metal data line layer and a second metal data line layer onto the substrate with the gate line assembly in a sequential manner;

forming a data line assembly with a predetermined pattern through etching the first metal data line layer and the second metal data line layer by using a second mask, the data line assembly including data lines, and source electrodes and drain electrodes;

etching the contact layer through the pattern of the data line assembly such that the contact layer has the same pattern as the data line assembly;

depositing a passivation layer onto the structured substrate such that the passivation layer covers the semiconductor layer and the data line assembly;

coating a photoresist film onto the passivation layer;

exposing the photoresist film to light by using a third mask, and developing the exposed photoresist film to form a photoresist pattern of partially different thickness;

forming a semiconductor pattern and contact windows, the semiconductor pattern being formed by etching the passivation layer and the underlying semiconductor layer at a pixel area defined by the neighboring gate line and data line through the

31. The method of claim 28 wherein the second layer has a light transmission control pattern of slits or mosaics.

32. The method of claim 28 wherein the first portion, the second portion and the third portion of the third mask are arranged to correspond respectively to the first portion, the second portion and the third portion of the photoresist pattern.

33. A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a gate insulating layer formed on the gate line assembly, the gate insulating layer having a first contact window exposing the gate pad, and an opening portion partially exposing the insulating substrate;

a semiconductor pattern formed on the gate insulating layer;

a contact pattern formed on the semiconductor pattern;

a data line assembly formed on the contact pattern with substantially the same outline as the contact pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrode while being separated from the source electrodes;

a passivation layer formed on the data line assembly with the same

outline as the semiconductor pattern except at portions of a second contact window exposing the data pad and a third contact window exposing the drain electrode;

a pixel electrode formed at a pixel area defined by the neighboring gate and data lines, the pixel electrode being electrically connected to the drain electrode through the third contact window while partially contacting the gate insulating layer; and

subsidiary gate and data pads contacting the gate and data pads, respectively.

34. The thin film transistor array substrate of claim 33 wherein the opening portion exposes the substrate between the pixel electrode and the neighboring data line.

35. The thin film transistor array substrate of claim 33 wherein the third contact window exposing the drain electrode is extended such that the borderline of the drain electrode is exposed to the outside.

36. A thin film transistor array substrate for a liquid crystal display comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer

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in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrodes while being separated from the source electrodes;

a second insulating layer formed on the data line assembly with the same outline as the semiconductor pattern, the second insulating layer having a second contact window exposing the gate pad through the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

37. The thin film transistor array substrate of claim 36 further comprising a contact layer formed between the semiconductor pattern and the data line assembly with the same outline as the data line assembly.

38. The thin film transistor array substrate of claim 36 further comprising supplemental gate pads and supplemental data pads covering the gate pad and the data pad, respectively.

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39. The thin film transistor array substrate of claim 36 further comprising a photo-interceptive organic pattern formed between the data line assembly and the overlying passivation layer.

40. The thin film transistor array substrate of claim 39 wherein the photo-interceptive pattern is provided with a fifth contact window exposing the drain electrode through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

41. The thin film transistor array substrate of claim 36 wherein the second insulating layer is formed of a photo-interceptive organic layer.

42. The thin film transistor array substrate of claim 41 wherein the first insulating layer has the same outline as the semiconductor pattern.

43. The thin film transistor array substrate of claim 42 wherein the opening width of the semiconductor pattern between the neighboring data lines is 1μ or more.

44. A thin film transistor array substrate for a liquid crystal display, comprising:

an insulating substrate;

a gate line assembly formed on the substrate, the gate line assembly having a plurality of gate lines proceeding in the horizontal direction, gate electrodes branched from the gate lines, and gate pads connected to end portions of the gate lines;

a first insulating layer formed on the gate line assembly, the first insulating layer having a first contact window exposing the gate pad;

a semiconductor pattern longitudinally formed on the first insulating layer in the vertical direction;

a data line assembly formed on the semiconductor pattern, the data line assembly having data lines proceeding in the vertical direction, source electrodes branched from the data lines, data pads connected to end portions of the data lines, and drain electrodes positioned opposite to the source electrodes with respect to the gate electrodes while being separated from the source electrodes, the data line assembly substantially having the same outline as the semiconductor pattern except the portion placed between the source electrode and the drain electrode;

a second insulating layer formed on the data line assembly, the second insulating layer having a second contact window exposing the first contact window, a third contact window exposing the data pad, and a fourth contact window exposing the drain electrode;

a color filter formed on the passivation layer at a pixel area defined by the neighboring gate and data lines; and

a pixel electrode formed on the color filter, the pixel electrode being connected to the drain electrode through the fourth contact window.

13 ~~45~~. The thin film transistor array substrate of claim 12 ~~44~~ further comprising a contact layer formed between the semiconductor pattern and the data line assembly substantially with the same outline as the data line assembly.

14 ~~46~~. The thin film transistor array substrate of claim 12 ~~44~~ further comprising supplemental gate pads and supplemental data pads covering the gate pads and the data pads, respectively.

47. The thin film transistor array substrate of claim 44 further comprising a photo-interceptive organic pattern formed on the passivation layer over the data line assembly and the gate line assembly.

48. The thin film transistor array substrate of claim 47 wherein the photo-interceptive organic pattern is provided with a fifth contact window exposing the drain electrode through the fourth contact window, the fifth contact window being narrower than the fourth contact window.

49. The thin film transistor array substrate of claim 44 wherein the second insulating layer is formed with a photo-interceptive organic layer.

50. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly on a substrate by using a first mask, the gate line assembly including gate lines, gate electrodes, and gate pads;

depositing a first insulating layer, a semiconductor layer, and a metal data line layer onto the substrate with the gate line assembly in a sequential manner;

forming a data line assembly with a predetermined pattern through etching the metal data line layer by using a second mask, the data line assembly including data lines, and source and drain electrodes;

depositing a second insulating layer onto the data line assembly;

forming contact windows exposing the drain electrode, the data pad, and the gate pad through selectively etching the second insulating layer and the underlying semiconductor layer and first insulating layer, and forming an opening portion exposing

photoresist pattern, a first contact window and a second contact window being formed by etching the passivation layer and the underlying second layers of the drain electrode and the data pad, a third contact window being formed by etching the passivation layer and the underlying semiconductor layer and gate insulating layer, and some upper portion of the gate pad;

removing the photoresist pattern; and

forming a pixel electrode by using a fourth mask such that the pixel electrode is connected to the drain electrode through the first contact window.

2. The method of claim 1, wherein the second metal data line layer is formed of aluminum or aluminum alloy.

3. The method of claim 2, wherein the first metal data line layer is formed of chrome, molybdenum, or molybdenum alloy.

4. The method of claim 1, wherein a supplemental data pad is formed in the step of forming the pixel electrode such that the supplemental data pad is connected to the first layer of the data pad through the second contact window.

5. The method of claim 1, wherein the gate line assembly is formed with a first metal gate line layer and a second metal gate line layer.

6. The method of claim 5, wherein the second layer of the gate pad is removed during in step of forming the gate line assembly.

7. The method of claim 6, wherein the second metal gate line layer is formed of aluminum or aluminum alloy.

8. The method of claim 7, wherein the first metal gate line layer is formed with chrome, molybdenum, or molybdenum alloy.

9. The method of claim 6, wherein a subsidiary gate pad is formed in the step of forming the pixel electrode such that the supplemental gate pad is connected to the first layer of the gate pad through the third contact window.

10. The method of claim 1, wherein the pixel electrode is formed of indium tin oxide or indium zinc oxide.

11. The method of claim 5, wherein the step of forming the semiconductor pattern and contact windows comprises the steps of:

exposing the gate pad through etching the passivation layer and the underlying semiconductor layer and gate insulating layer, and exposing the data pad through etching the passivation layer;

exposing the passivation layer positioned over the drain electrode and at the pixel area;

exposing the drain electrode while forming the semiconductor pattern through etching the exposed portions of the passivation layer at the pixel area and the underlying semiconductor layer; and

forming the first contact window, the second contact window and the third contact window through etching the second layers of the drain electrode, the data pad, and the gate pad.

12. The method of claim 11, wherein the second layers of the drain electrode, the gate pad and the data pad is wet-etched.

13. The method of claim 11, wherein the second layers of the drain electrode, the gate pad and the data pad is dry-etched.

14. The method of claim 11, wherein the passivation layer positioned over the drain electrode and at the pixel area is exposed by removing the photoresist film over the passivation layer through oxygen-based ashing.

15. The method of claim 14, wherein N_6 or Ar is used for the oxygen-based ashing.

16. The method of claim 1, wherein the step of forming the semiconductor pattern and contact windows comprises the steps of:

exposing the second layers of the drain electrode and the data pad through etching the passivation layer, and exposing the second layer of the gate pad through etching the passivation layer and the underlying semiconductor layer and gate insulating layer;

exposing the first layers of the drain electrode, the data pad and the gate pad through etching the exposed portions of the second layers of the drain electrode, the data pad and the gate pad;

exposing the portion of the passivation layer adjacent to the removed portion of the passivation layer over the drain electrode, and the portion of the passivation layer positioned at the pixel area; and

forming the semiconductor pattern through etching the exposed portion of the passivation layer at the pixel area, and forming the first contact window through etching the exposed portion of the passivation layer adjacent to the removed portion of

the passivation layer over the drain electrode while exposing the second layer of the drain electrode.

17. The method of claim 16, wherein the portion of the passivation layer adjacent to the removed portion of the passivation layer over the data pad is exposed in the step of exposing the portion of the passivation layer adjacent to the removed portion of the passivation layer over the drain electrode, and the second contact window is formed during the step of forming the first contact window through etching the exposed portion of the passivation layer over the data pad while exposing the second layer of the data pad.

18. The method of claim 16, wherein the exposed portions of the second layers of the drain electrode, the data pad and the gate pad is wet-etched.

19. The method of claim 16, wherein the etching with respect to the exposed portions of the second layers of the drain electrode, the data pad and the gate pad is performed by using a dry-etching technique.

20. The method of claim 16, wherein the step of exposing the portion of the passivation layer adjacent to the removed portion of the passivation layer over the drain electrode, and the portion of the passivation layer positioned at the pixel area, is performed by removing the photoresist film over the passivation layer through oxygen-based ashing.

21. The method of claim 1, wherein the semiconductor layer is formed of amorphous silicon.

22. The method of claim 21, wherein the contact layer is formed of phosphorous-doped amorphous silicon.

23. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly on a substrate by using a first mask, the gate line assembly including gate lines, gate electrodes, and gate pads;

depositing a gate insulating layer, a semiconductor layer, a contact layer, and a first metal data line layer and a second metal data line layer onto the substrate with the gate line assembly in a sequential manner;

forming a data line assembly with a predetermined pattern through etching the first metal data line layer and the second metal data line layer by using a second mask, the data line assembly including data lines, and source and drain electrodes;

etching the contact layer through the pattern of the data line assembly such that the contact layer has the same pattern as the data line assembly;

depositing a photosensitive passivation layer onto the structured substrate such that the photosensitive passivation layer covers the semiconductor layer and the data line assembly;

exposing the photosensitive passivation layer to light by using a third mask, and developing the exposed passivation layer to form a passivation patternpassivation having partially different thickness such that the passivation pattern comprises a first portion with no thickness, thus exposing the semiconductor layer over the gate pad, a first contact window and the second contact window and exposing the

drain electrode and data pad, a second portion with a first thickness positioned adjacent to the first and second contact windows and at a pixel area defined by the neighboring gate and data lines, and a third portion with a second thickness, the second thickness being greater than the first thickness;

forming a third contact window exposing the gate pad by etching the semiconductor layer and the underlying gate insulating layer through the first portion of the passivation pattern;

removing the second layers of the drain electrode, the data pad and the gate pad through the first contact window, the second contact window and the third contact window;

ashing the second portion of the passivation pattern to expose the semiconductor layer at the pixel area, and increase the width of the first and second contact windows;

forming a semiconductor pattern by etching the exposed semiconductor layer at the pixel area; and

forming a pixel electrode such that the pixel electrode is electrically connected to the drain electrode through the first contact window.

24. The method of claim 23 wherein a supplemental data pad and a supplemental gate pad are formed during the step of forming the pixel electrode such that the supplemental data and gate pads contact the first layers of the data and gate pads through the second and third contact windows, respectively.

25. The method of claim 23 wherein the passivation layer is formed of an organic insulating material.

26. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly on a substrate by using a first mask, the gate line assembly including gate lines, gate electrodes, and gate pads;

depositing a gate insulating layer, a semiconductor layer, a contact layer, and a metal data line layer onto the substrate with the gate line assembly in a sequential manner;

forming a data line assembly with a predetermined pattern through etching the metal data line layer by using a second mask, the data line assembly including data lines, and source and drain electrodes;

etching the contact layer through the pattern of the data line assembly such that the contact layer has the same pattern as the data line assembly;

depositing a passivation layer onto the structured substrate such that the passivation layer covers the semiconductor layer and the data line assembly;

coating a photoresist film onto the passivation layer;

exposing the photoresist film to light by using a third mask, and developing the exposed photoresist film to thereby form a photoresist pattern, the photoresist pattern being partially differentiated in thickness such that the photoresist pattern has a first portion with no thickness positioned over the gate and data pads and between a pixel area and the neighboring data line, a second portion with a first thickness positioned over the drain electrode and the pixel area, and a third portion with a second thickness, the second thickness being greater than the first thickness;

forming a semiconductor pattern, contact windows and an opening portion, the semiconductor pattern being formed by etching the passivation layer and the underlying semiconductor layer at the pixel area through the photoresist pattern, the first contact window and the second contact windows being formed by etching the passivation layer over the drain electrode and the data pad, the third contact window being formed by etching the passivation layer and the underlying semiconductor layer and gate insulating layer over the gate pad, the opening portion being formed by etching the passivation layer and the underlying semiconductor layer and gate insulating layer between the pixel area and the data line;

removing the photoresist pattern; and

forming a pixel electrode by using a fourth mask such that the pixel electrode is connected to the drain electrode through the first contact window.

27. The method of claim 26 wherein the step of forming the semiconductor pattern, contact windows and the opening portion comprises the steps of:

etching the passivation layer and the underlying semiconductor layer and gate insulating layer over the gate pad while partially leaving the gate insulating layer, etching the passivation layer over the data pad to form the second contact window, and etching the passivation layer and the underlying semiconductor layer and gate insulating layer between the pixel area and the data line while partially leaving the gate insulating layer;

exposing the passivation layer positioned over the drain electrode and at the pixel area;

etching the passivation layer over the drain electrode to form the first

contact window while removing the passivation layer at the pixel area, removing the gate insulating layer remaining over the gate pad to form the third contact window, and removing the gate insulating layer remaining between the pixel area and the data line to form the opening portion; and

etching the semiconductor layer at the pixel area to form the semiconductor pattern.

28. The method of claim 26 wherein the third mask for forming the photoresist pattern comprises:

a transparent substrate;

a first layer formed on the transparent substrate, the first layer having a light transmissivity lower than the substrate; and

a second layer formed on the transparent substrate while overlapping with the first layer, the second layer having a light transmissivity different from the light transmissivity of the substrate and the first layer;

wherein the transparent substrate comprises a first portion without the first layer and the second layer, a second portion with the first layer only, and a third portion with both the first layer and the second layer.

29. The method of claim 28 wherein the transparent substrate has a light transmissivity of 90%, the first layer has a light transmissivity of 20-40%, and the second layer has a light transmissivity of 3% or less.

30. The method of claim 28 wherein the first layer has a light transmission control pattern of slits or mosaics.

the first insulating layer through selectively etching the second insulating layer and the underlying semiconductor layer at a pixel area defined by the neighboring gate and data lines;

forming a color filter on the first insulating layer at the pixel area through the opening portion; and

forming a pixel electrode on the color filter.

51. The method of claim 50 wherein a contact layer is further deposited onto the semiconductor layer during the step of depositing the metal data line layer, and the contact layer is etched together with the metal data line layer during the step of forming the data line assembly.

52. The method of claim 51 wherein the step of forming contact windows and the opening portion comprises the steps of:

depositing a photoresist film onto the second insulating layer;

exposing the photoresist film to light through a third mask, the third mask being differentiated in light transmissivity at three or more portions.

developing the exposed photoresist film to form a photoresist pattern; and

selectively etching the second insulating layer, the contact layer, the semiconductor layer and the first insulating layer with the photoresist pattern.

53. The method of claim 50 further comprising the step of forming a photo-interceptive organic pattern after the step of forming contact windows and the opening portion.

54. The method of claim 50 wherein the second insulating layer is formed of a photo-interceptive organic layer.

55. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly on a substrate by using a first mask, the gate line assembly including gate lines, gate electrodes, and gate pads;

depositing a first insulating layer, a semiconductor layer, a metal data line layer onto the substrate with the gate line assembly in a sequential manner;

forming a data line assembly with data lines, and source and drain electrodes through etching the metal data line layer by using a second mask, and a semiconductor pattern through etching the semiconductor layer except the portion of the semiconductor layer placed at a channel region between the source and drain electrodes;

depositing a second insulating layer onto the data line assembly, the second insulating layer having contact windows exposing the drain electrode, the data pad and the gate pad;

forming a color filter at a pixel area defined by the neighboring gate and data lines; and

forming a pixel electrode on the color filter such that the pixel electrode is connected to the drain electrode through the first contact window.

56. The method of claim 55 wherein a contact layer is further deposited onto the semiconductor layer during the step of depositing the metal data line layer, and the contact layer is etched together with the metal data line layer and semiconductor layer

during the step of forming the data line assembly to form a contact pattern with substantially the same outline as the data line assembly.

57. The method of claim 56 wherein the step of forming the data line assembly, the semiconductor pattern and the contact pattern comprises the steps of:

depositing a photoresist film onto the metal data line layer;

exposing the photoresist film to light through a third mask, the third mask having different light transmissivities at three or more portions.

developing the exposed photoresist film to form a photoresist pattern; and

selectively etching the metal data line layer, the contact layer, the semiconductor layer with the photoresist pattern.

58. The method of claim 55, further comprising the step of forming a photo-interceptive organic pattern after the step of forming the data line assembly and the semiconductor pattern.

59. The method of claim 55, wherein the second insulating layer is formed of a photo-interceptive organic layer.

60. A method for fabricating a thin film transistor array substrate for a liquid crystal display, comprising the steps of:

forming a gate line assembly on a substrate by using a first mask, the gate line assembly including gate lines, gate electrodes, and gate pads;

depositing a first insulating layer, a semiconductor layer, a metal data line layer onto the substrate with the gate line assembly in a sequential manner;

forming a data line assembly with a predetermined pattern through etching the metal data line layer by using a second mask, the data line assembly including data lines, and source and drain electrodes;

depositing a second insulating layer onto the data line assembly;

forming contact windows exposing the drain electrode, the data pad, and the drain electrode, and an opening portion exposing the substrate and the gate line through etching the second insulating layer and the underlying semiconductor layer and first insulating layer between the neighboring data lines;

forming a color filter on the exposed portion of the substrate and the gate line through the opening portion; and

forming a pixel electrode on the color filter.

61. The method of claim 60, wherein a contact layer is further deposited onto the semiconductor layer during the step of depositing the metal data line layer, and the contact layer is etched together with the metal data line layer during the step of forming the data line assembly.

62. The method of claim 60 wherein the second insulating layer is formed of a photo-interceptive organic layer.